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FIG. I

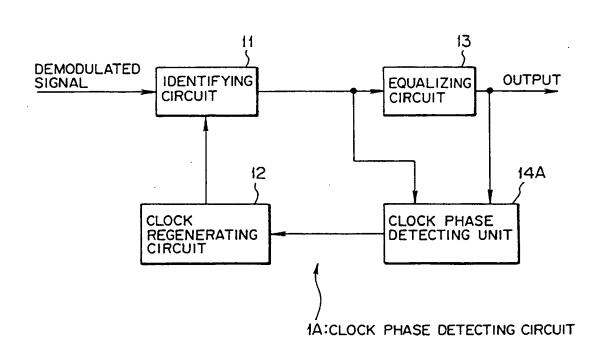


FIG. 2

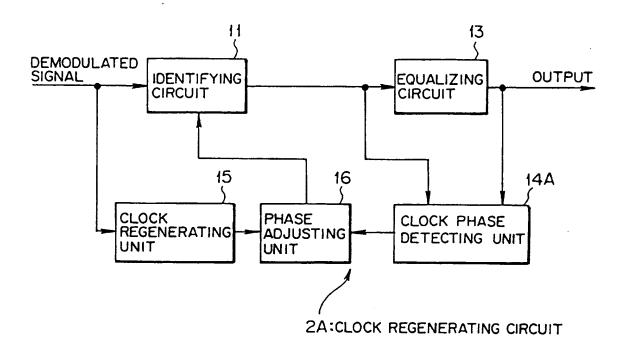
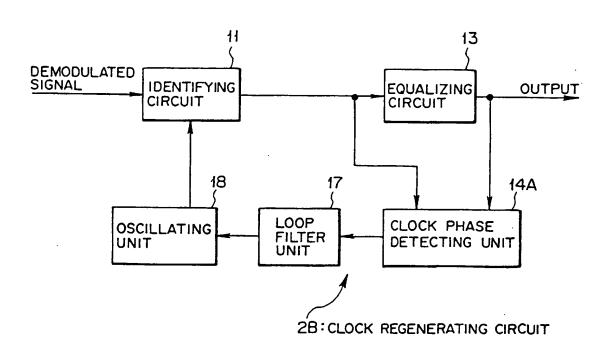


FIG.3



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FIG.4

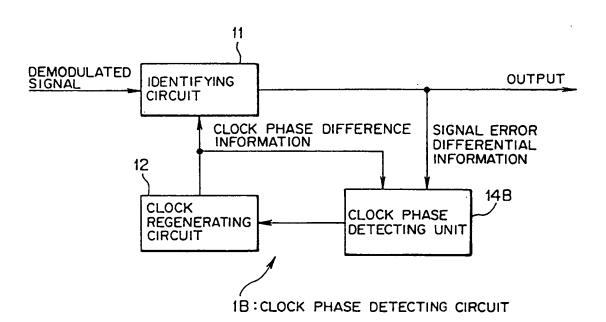




FIG.5

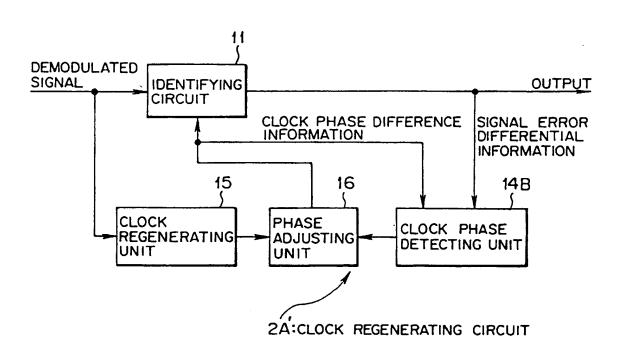
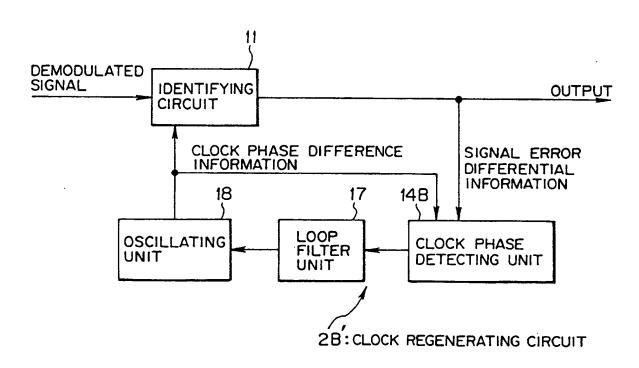
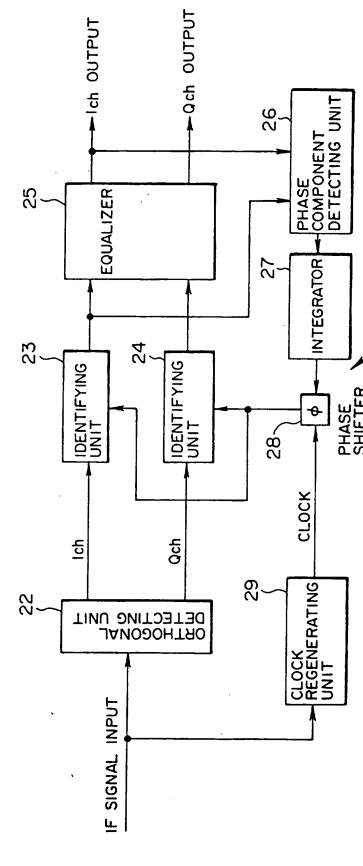


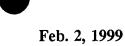
FIG.6

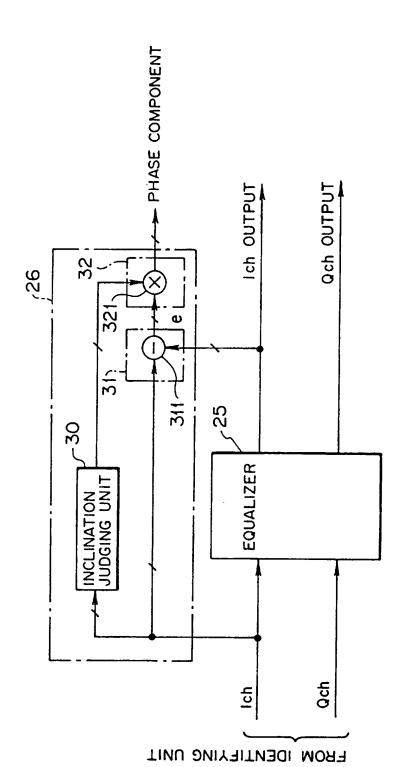


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35

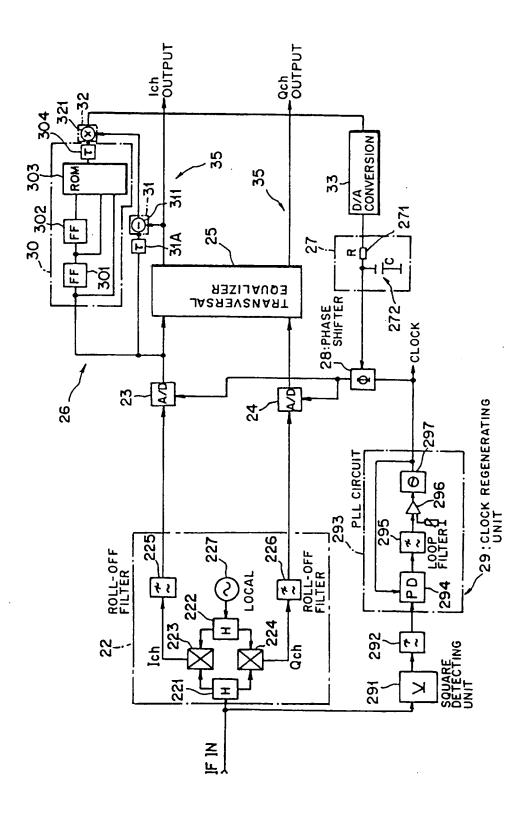






F16.8

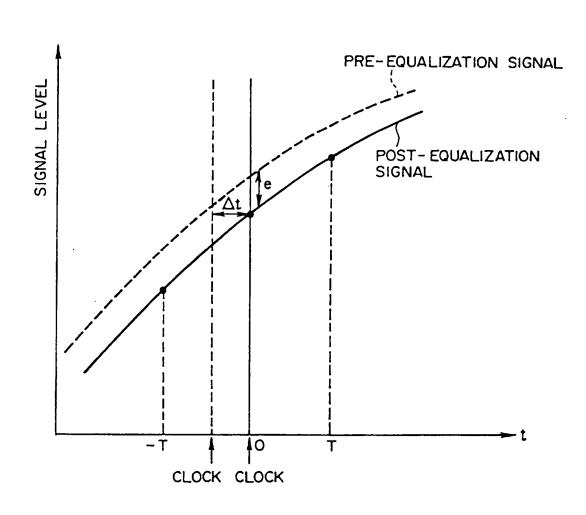




6 9 :

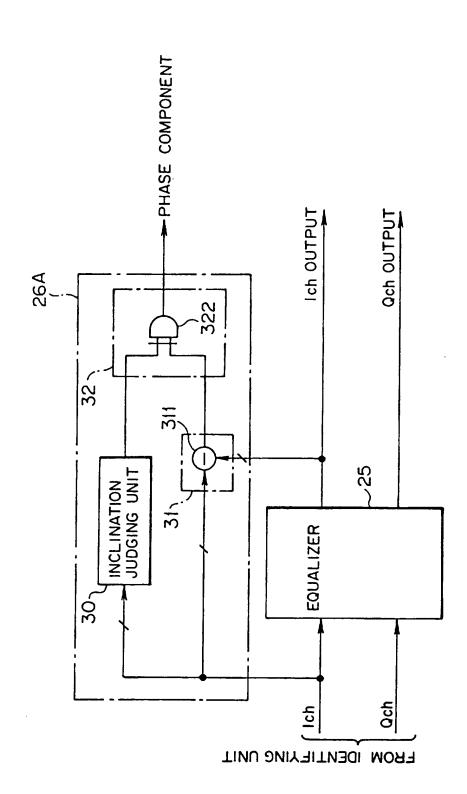


FIG. 10



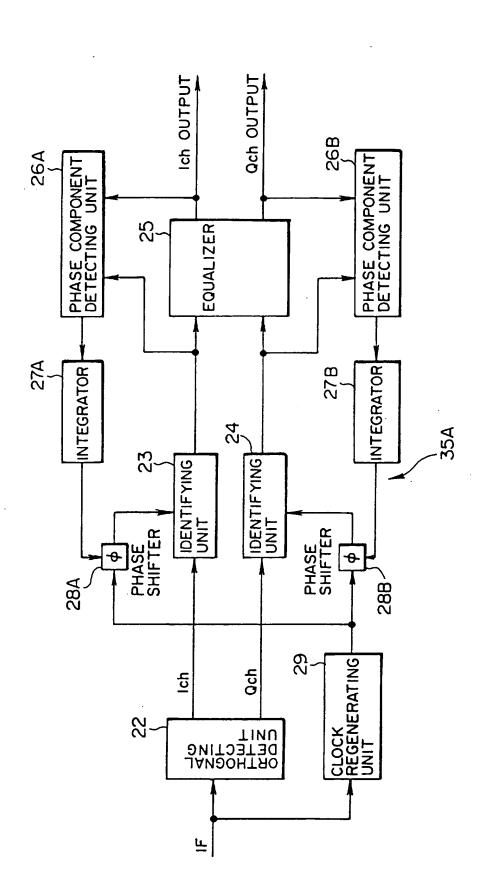
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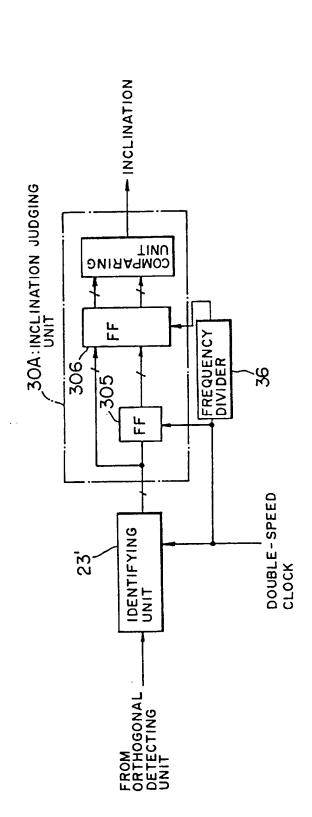
F16. 12



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QCh OUTPUT 35B 302 TRANSVERSAL EQUALIZER CLOCK / 301 29:CLOCK REGENERATING UNIT PHASE SHIFTER 28B ROLL-OFF £ }

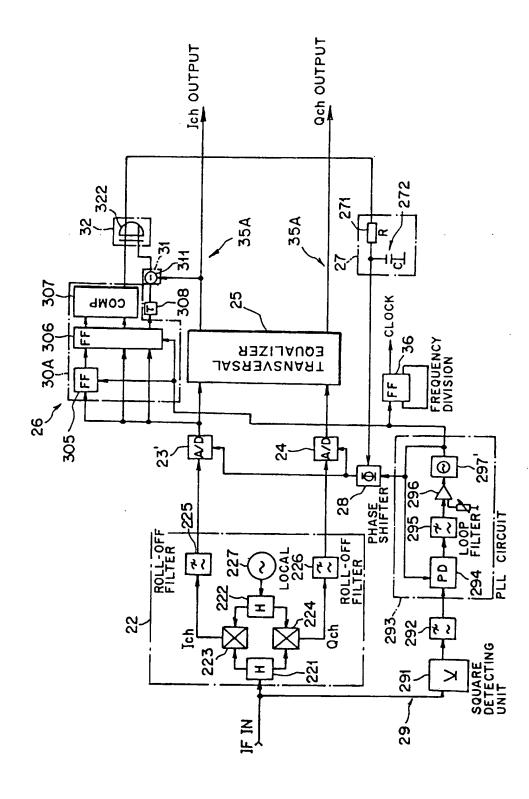
F16.14



F16.15



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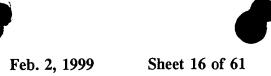
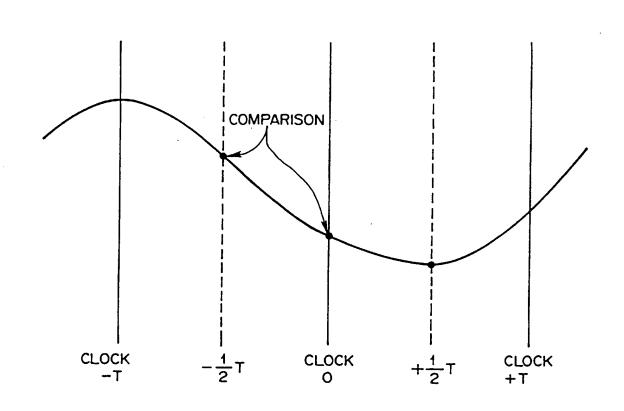


FIG.16



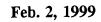
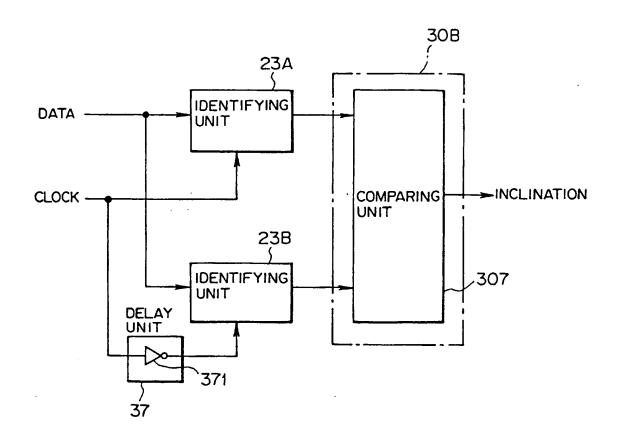
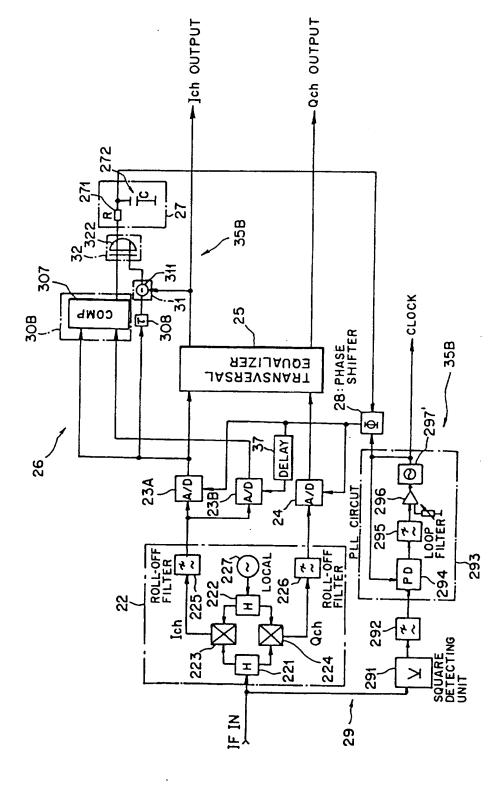


FIG.17



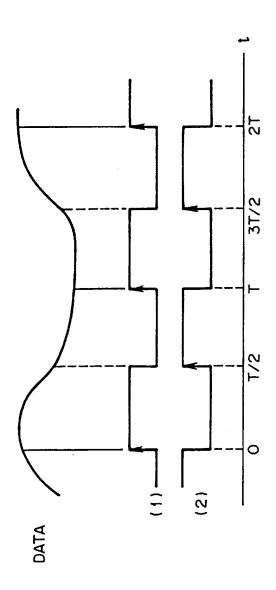


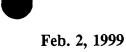
hoot 19 of 61



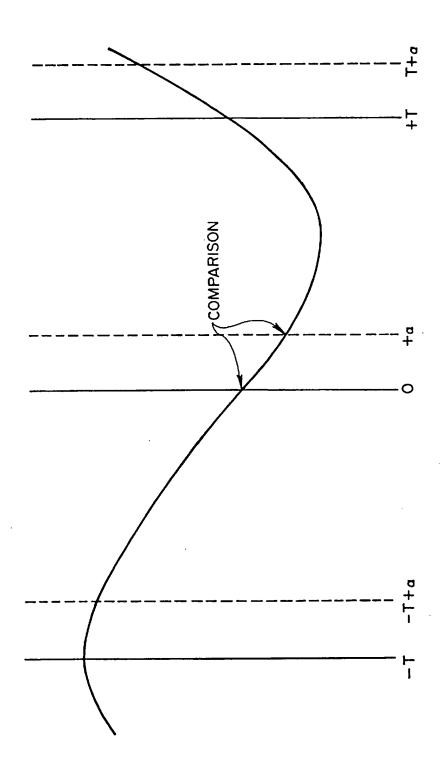
F | G. | 18







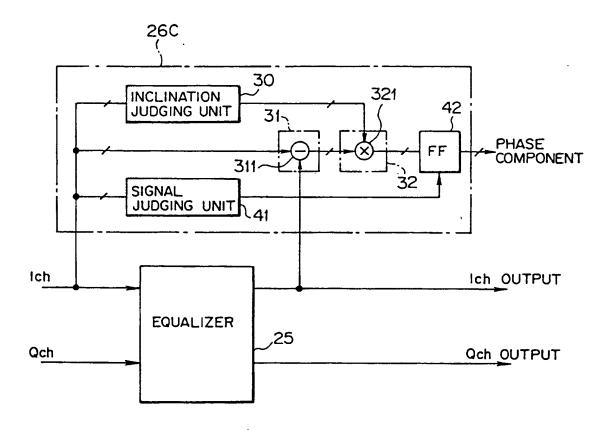




F 1 G. 20



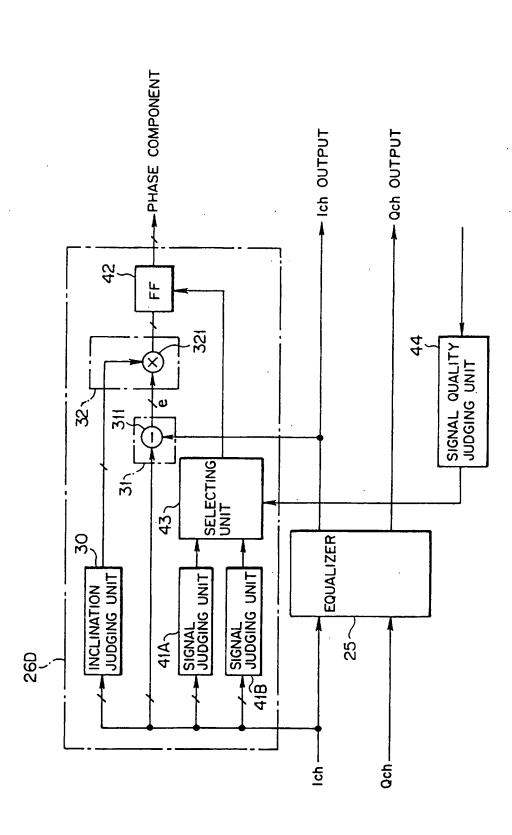
FIG.21





-Ich OUTPUT - ach OUTPUT 35C 33 TRANSVERSAL EQUALIZER **26C** 29: CLOCK REGENERATING UNIT / 293 ROLL-OFF FILTER 25-



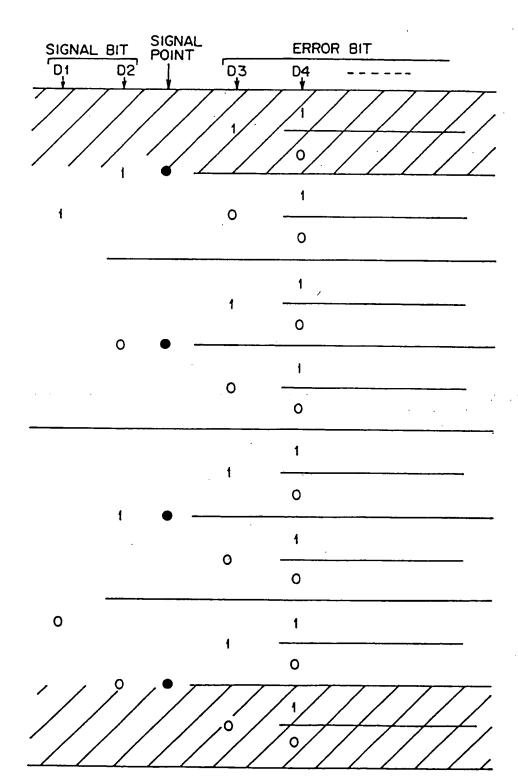


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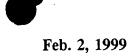
- ach OUTPUT ► Ich OUTPUT FRAME SYNCHRONIZATION CIRCUIT(ERROR CORRECTION, ETC, 304 SYNCHRONIZATION SIGNAL ROM TRANSVERSAL EQUALIZER SIGNAL JUDGING: 41B-UNIT SIGNAL JUDGING: 41A UNIT 26D 23 ROLL-OFF FILTER 25 ე წ 292 53

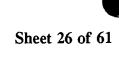


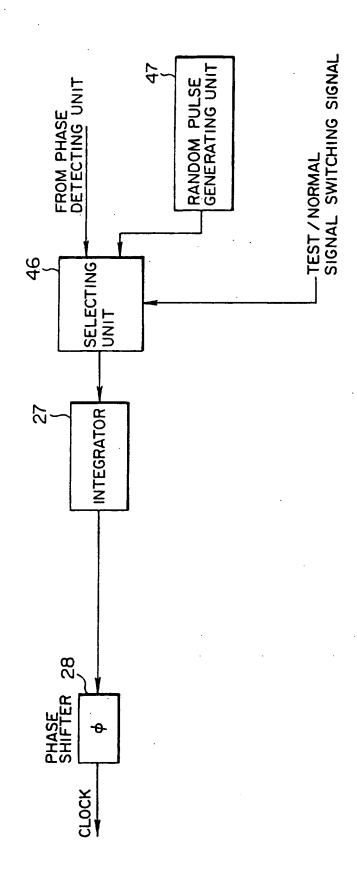


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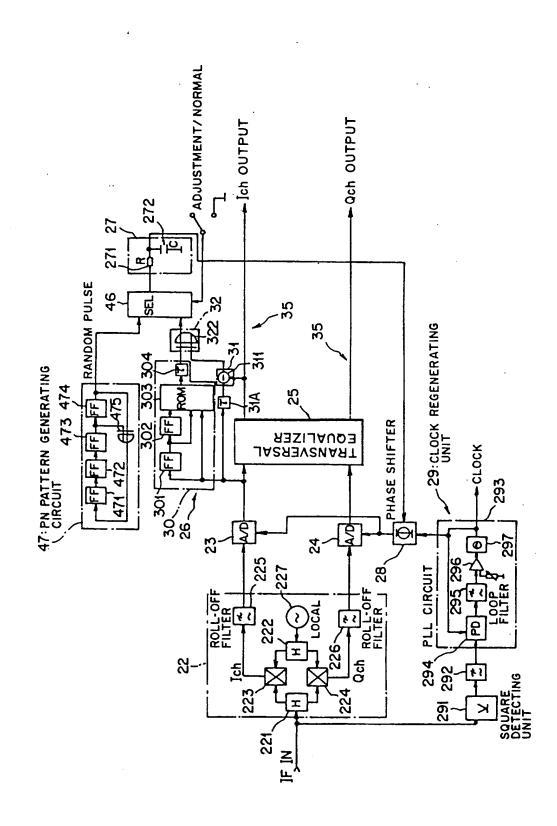




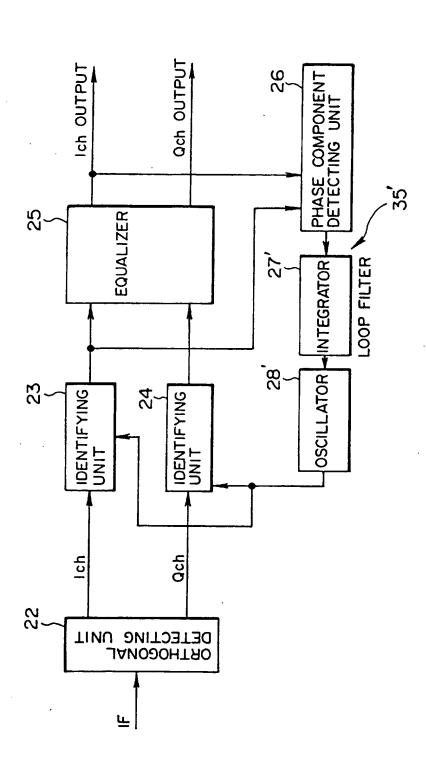
F16.26



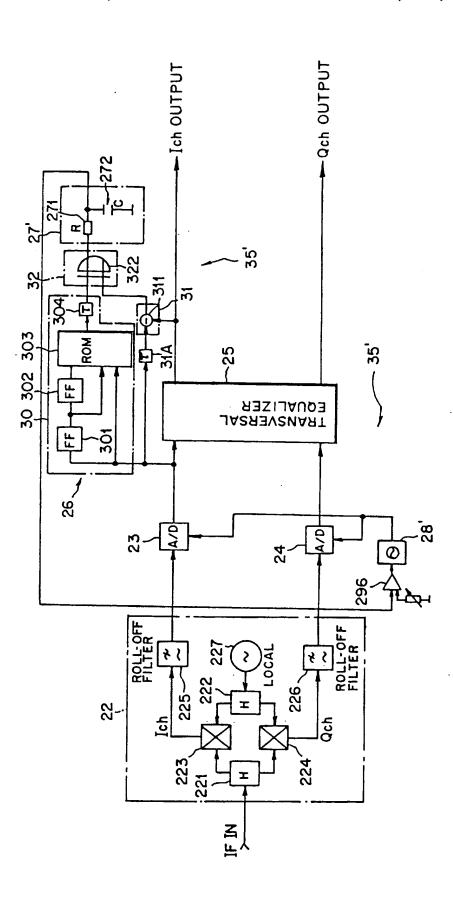
F 1 G. 27





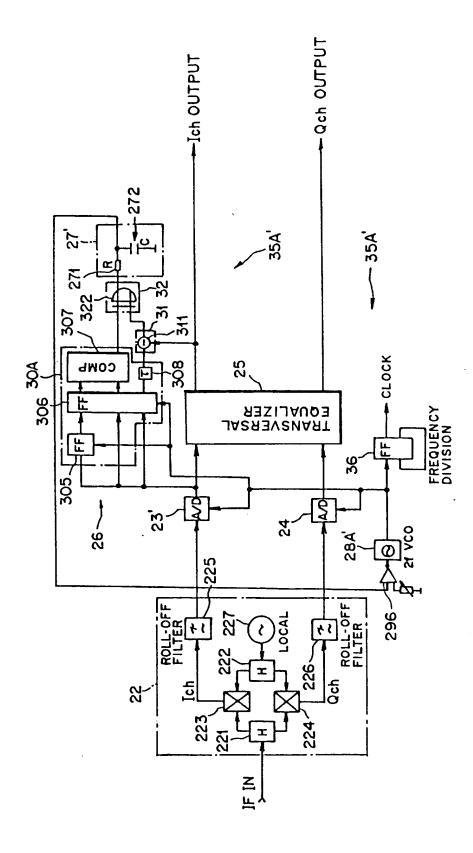


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. I G. 29





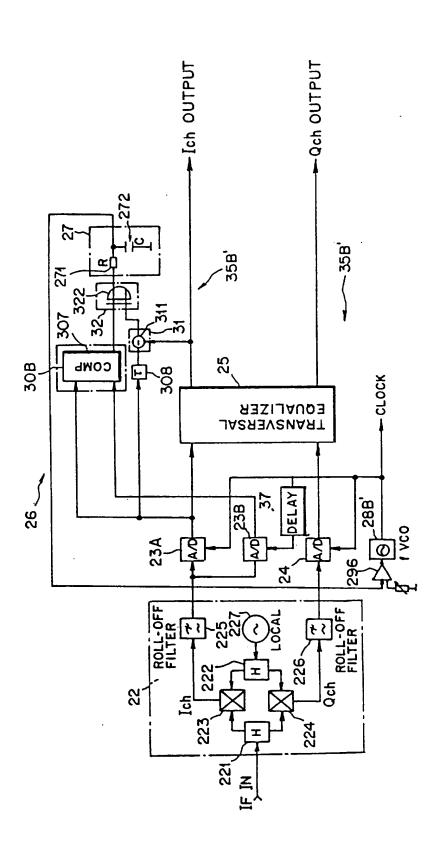


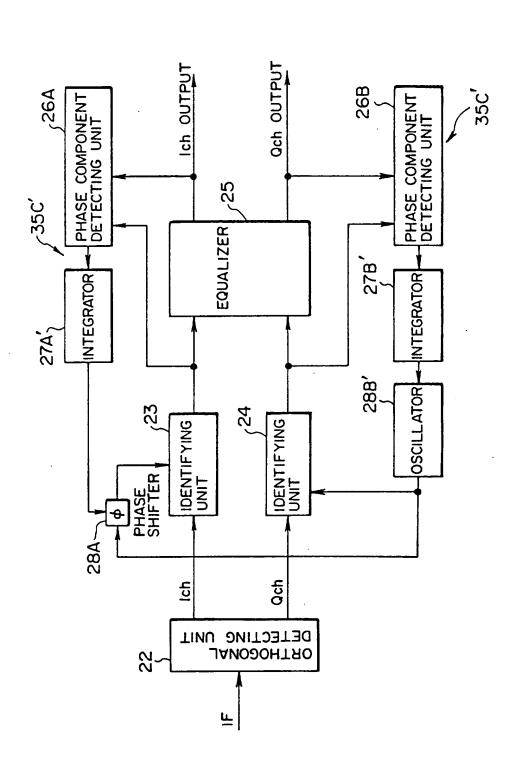


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F 1 G. 3

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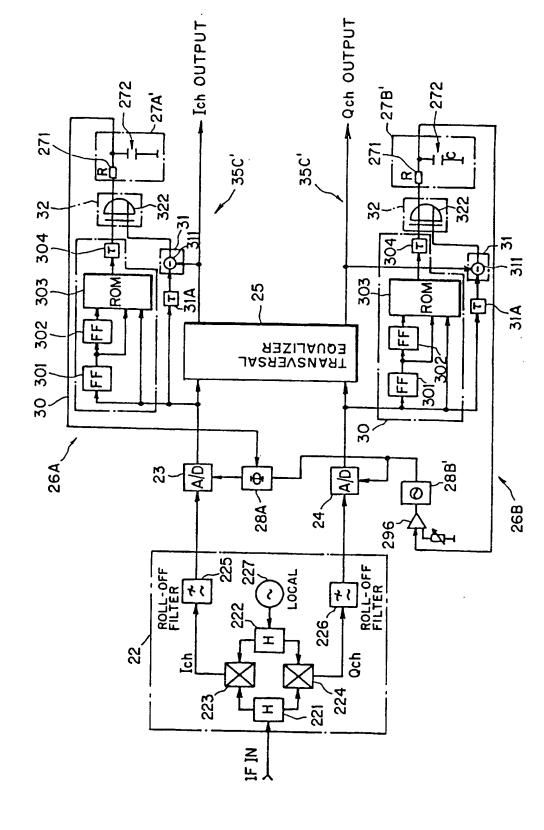


F16.32

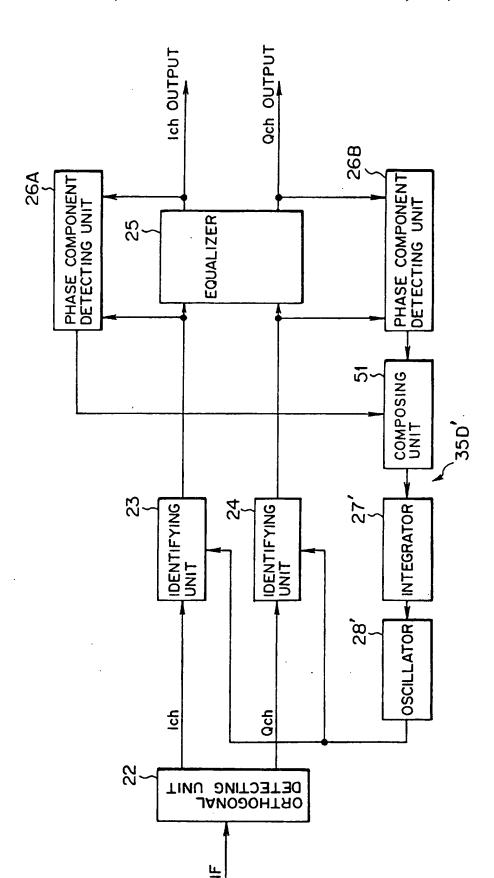
F16.33



Shoot 33 of 61



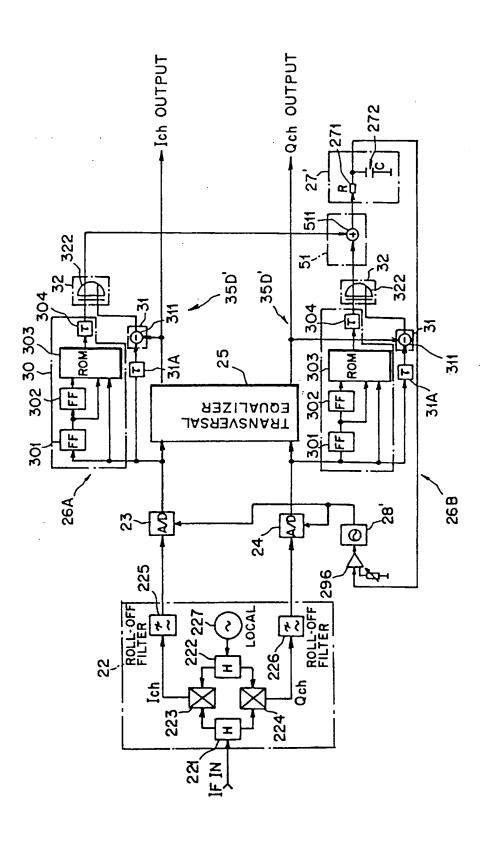




6.34

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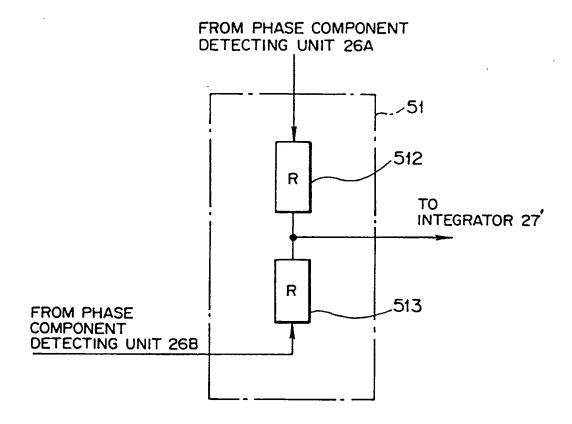
F16.35

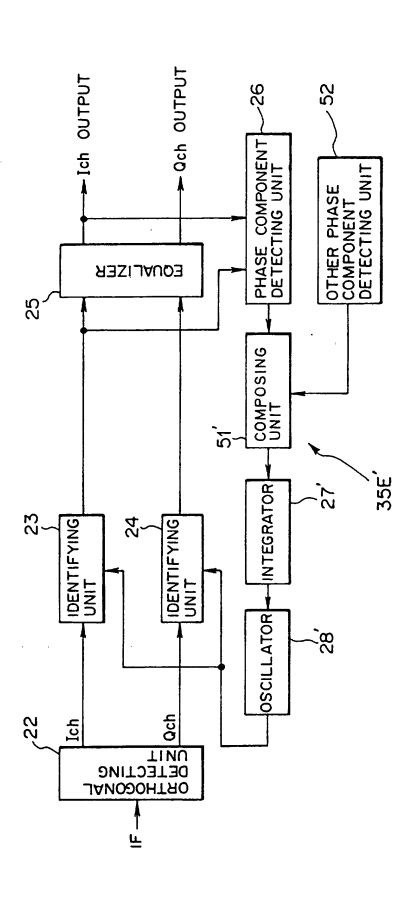


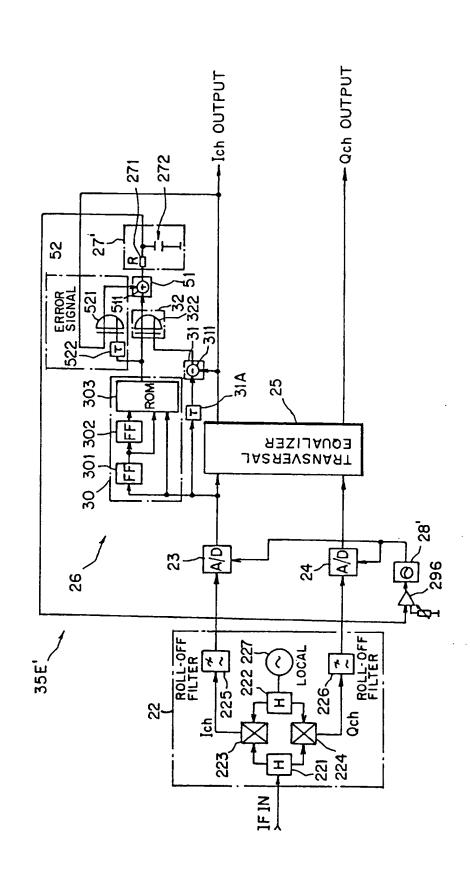


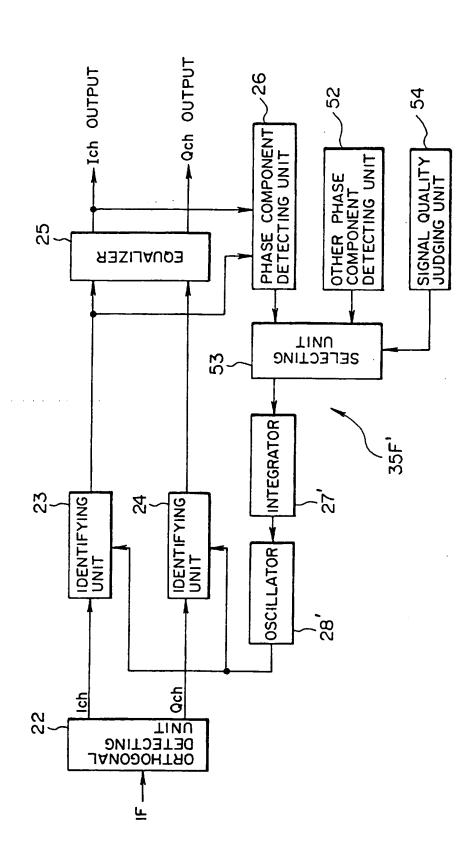
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FIG. 36

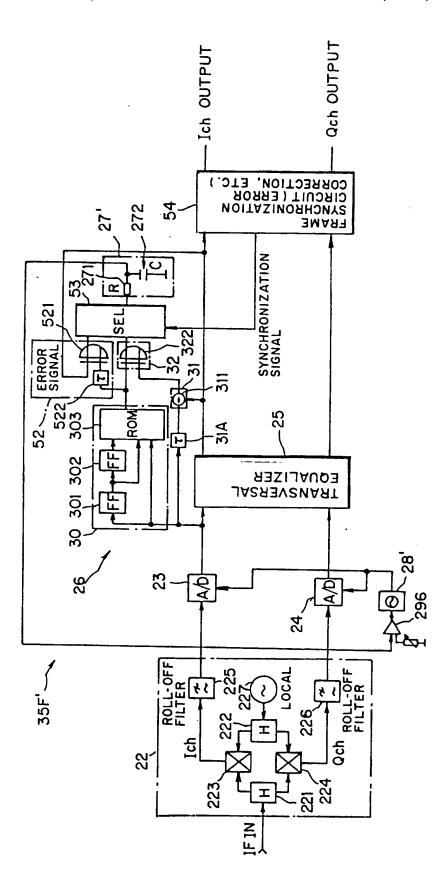








F16. 40



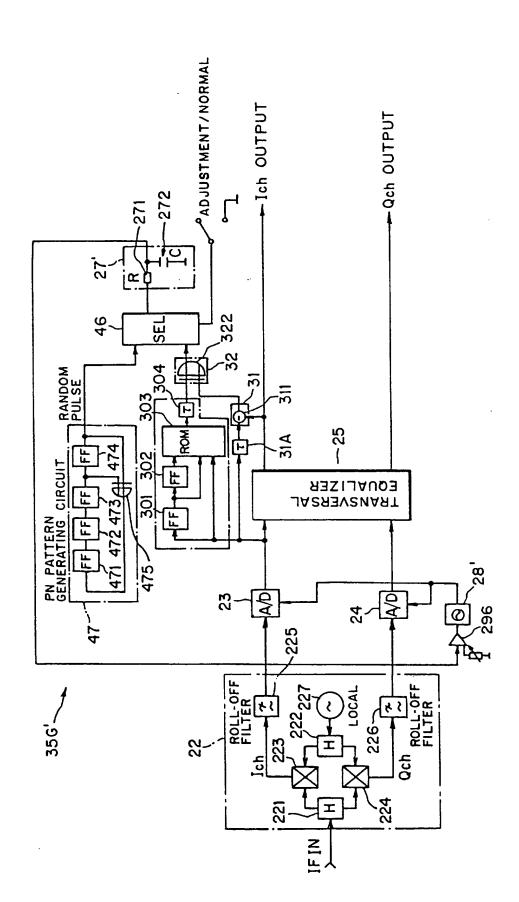
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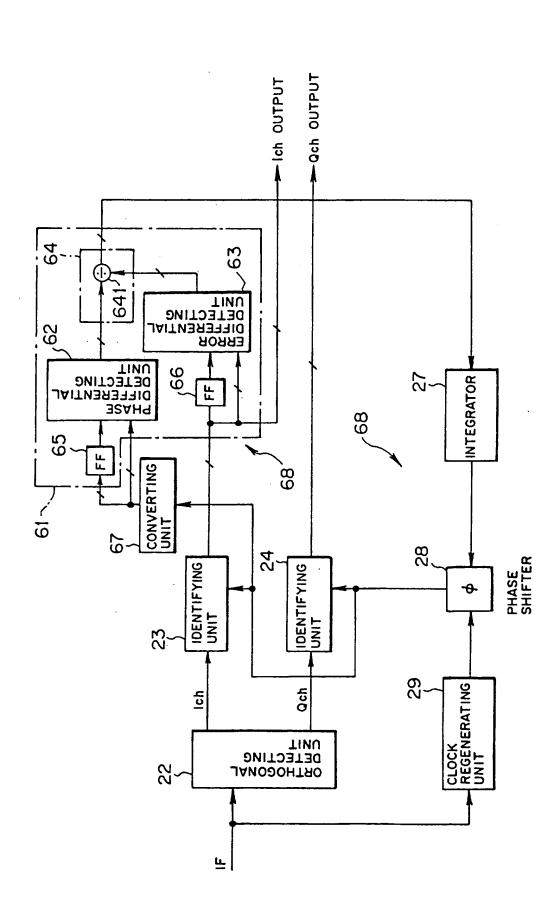
TEST/NORMAL SWITCHING SIGNAL SELECTING UNIT INTEGRATOR 296 , 78,

F16.4

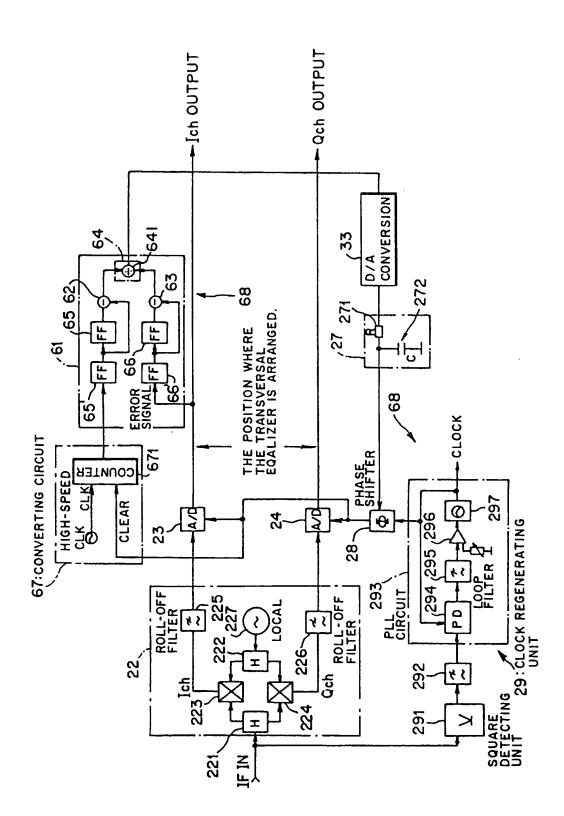
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F 1 G. 44





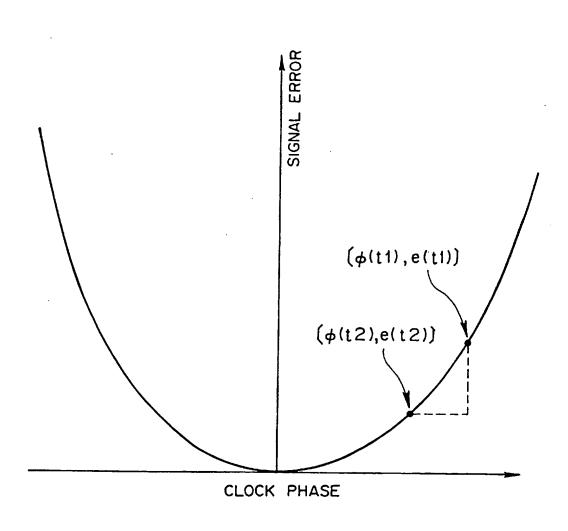
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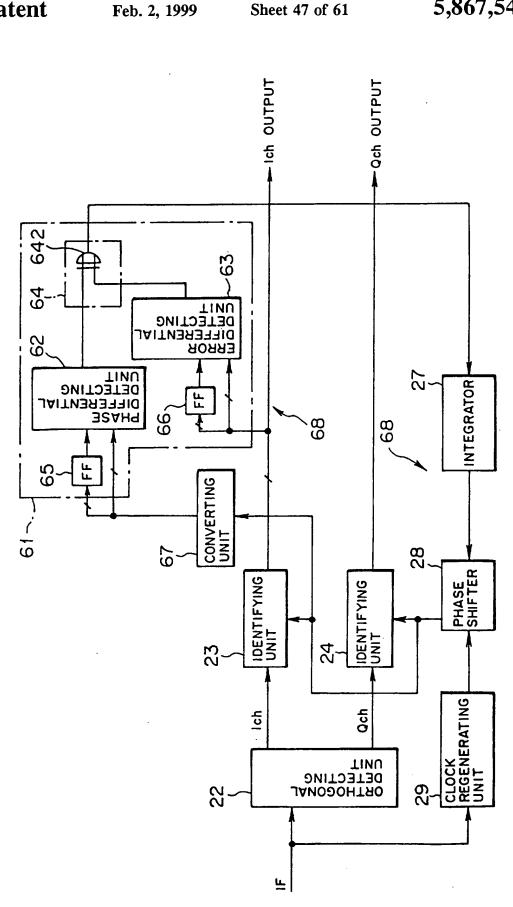
FIG. 45

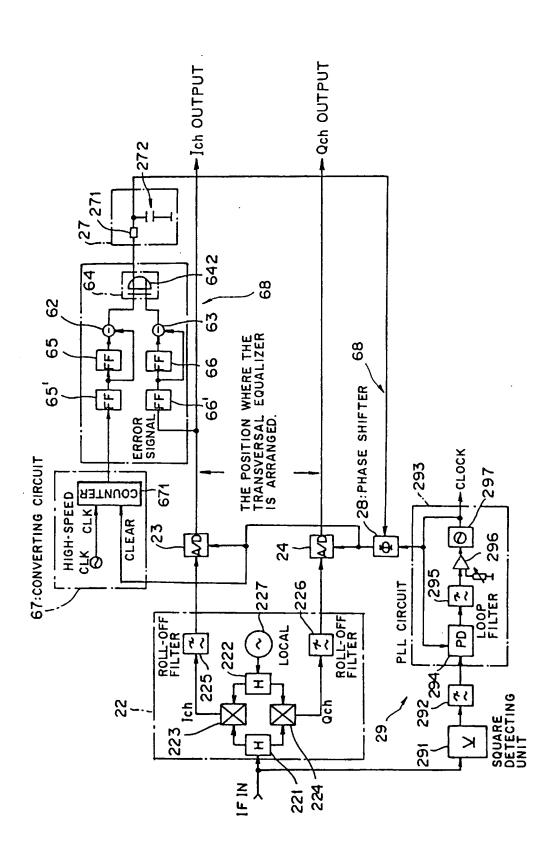
SIGNAL	BIT	SIGNAL		ERROR BIT
D1	DS	SIGNAL POINT 5	D3	D4
1	1	•	1 -	1
				0
			0 -	1
				0
	0	•	0 -	. 1
				0
			o –	1
				0
0	1	•	1 -	1
				0
			0 -	1
				0
	0	•	1 —	1
				0
			0 —	1
				0



FIG.46







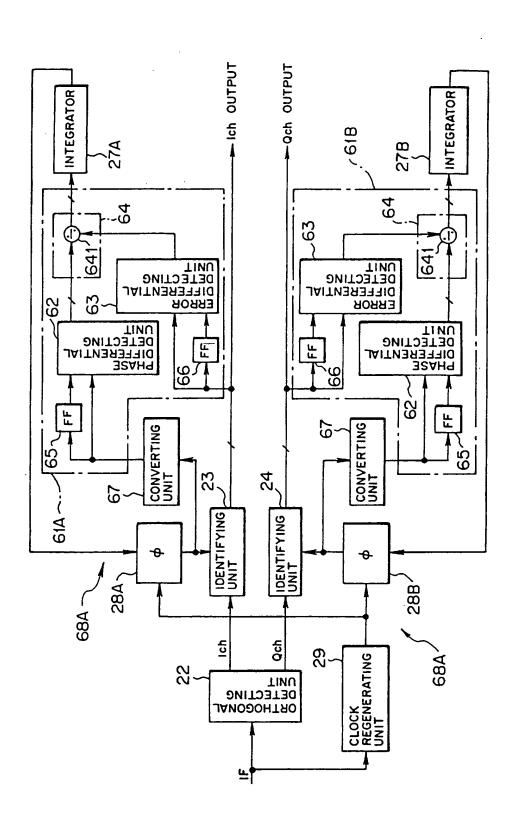
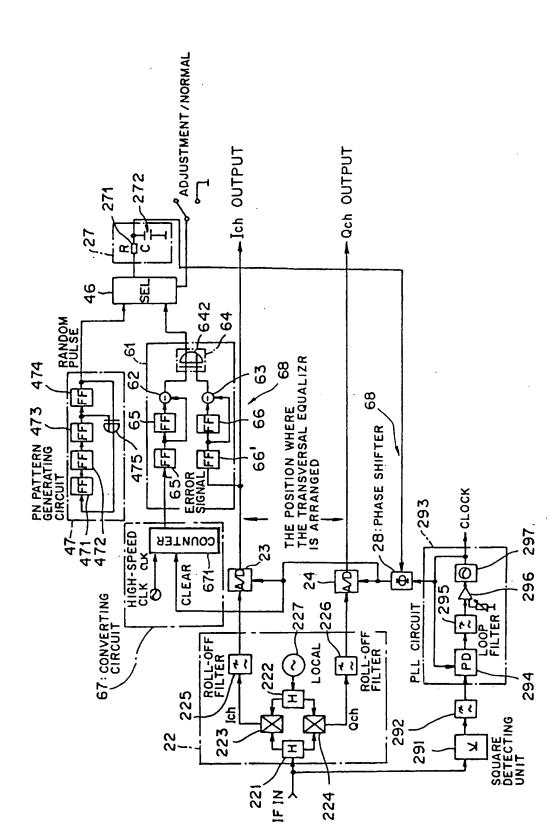
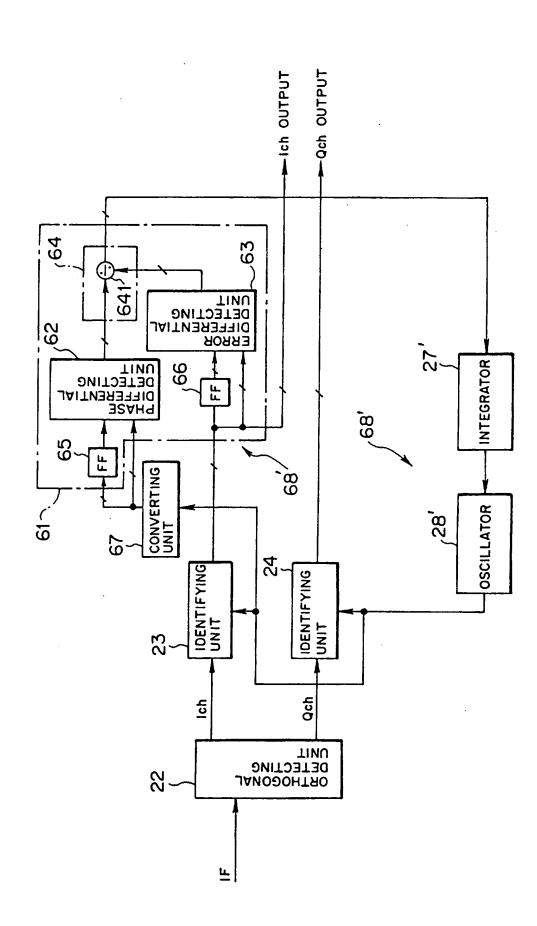


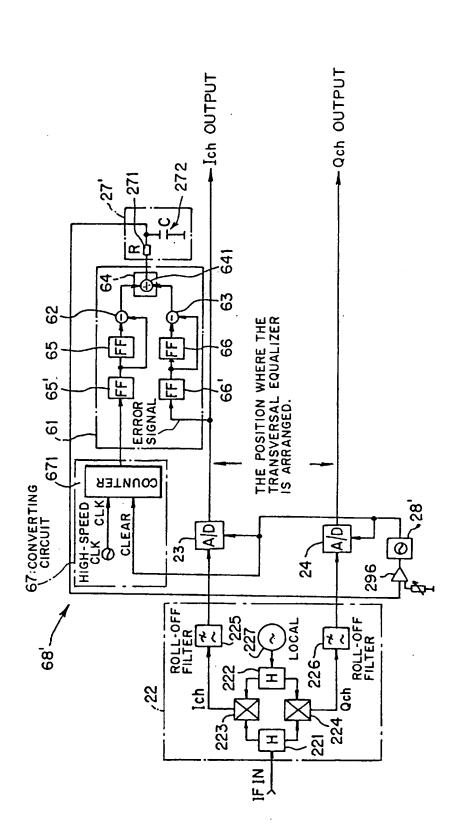
FIG. 49

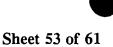
F16. 50





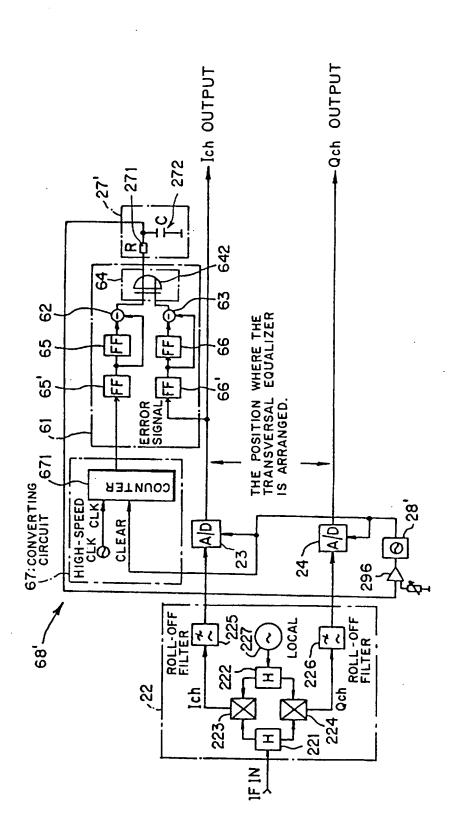
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COVILDED OTHOR



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-Qch OUTPUT 641 62 65, 10 , 67 67:CONVERTING (CIRCUIT ROLL-OFF FILTER

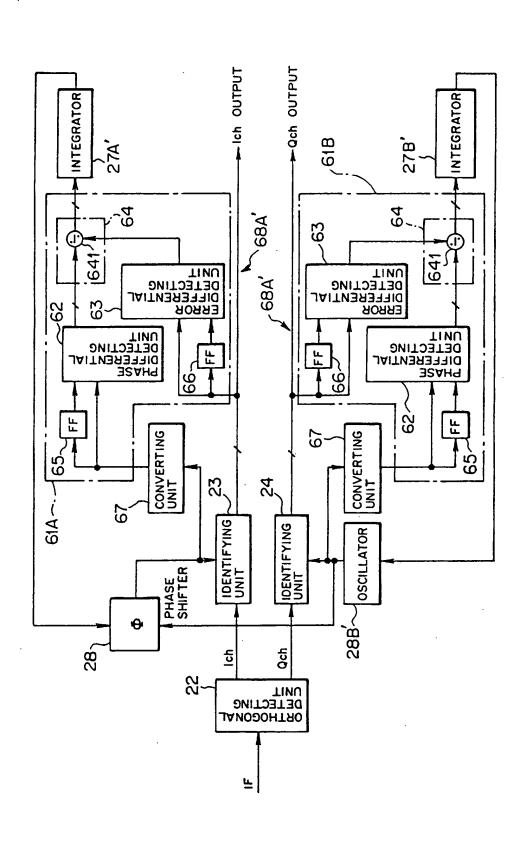
F16. 54

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-ICH OUTPUT 61B 64 68A' 63 641 641 ERROR DIFFERENTIAL DETECTING UNIT ERROR OIFFERENTIAL DETECTING UNIT 68A' 82 63 PHASE OIFFERENTIAL OETECTING UNIT PHASE OIFFERENTIAL DETECTING UNIT 14 661 62 L. FF CONVERTING CONVERTING 65~ 657 24 23 61A~ IDENTIFYING UNIT IDENTIFYING UNIT COMPOSING 9 INTEGRATOR 25 ORTHOGONAL DETECTING UNIT OSCILLATOR ഥ

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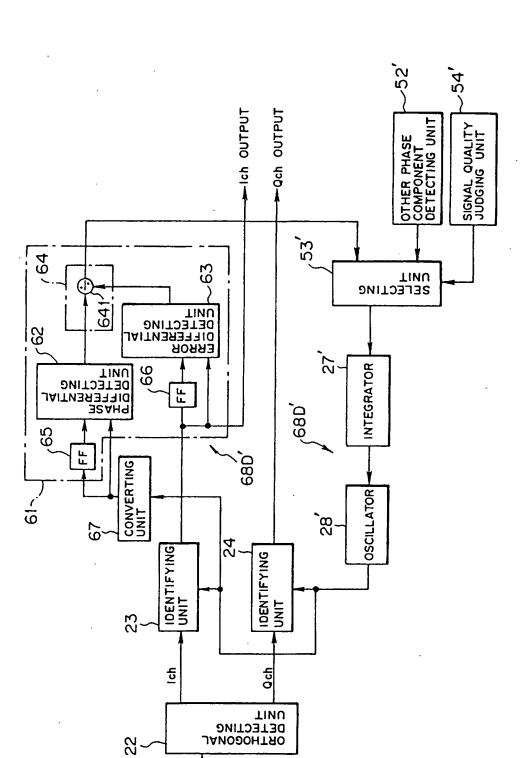


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52, -Och OUTPUT -Ich OUTPUT COMPOSING 64 63 641 ERROR DIFFERENTIAL DETECTING UNIT 62 PHASE OIFFERENTIAL DETECTING UNIT INTEGRATOR FF 65 ¥ CONVERTING UNIT , 980 OSCILLATOR 61) **67** IDENTIFYING UNIT 4 IDENTIFYING UNIT 23 당 S ORTHOGONAL DETECTING UNIT 뜨

F16.57

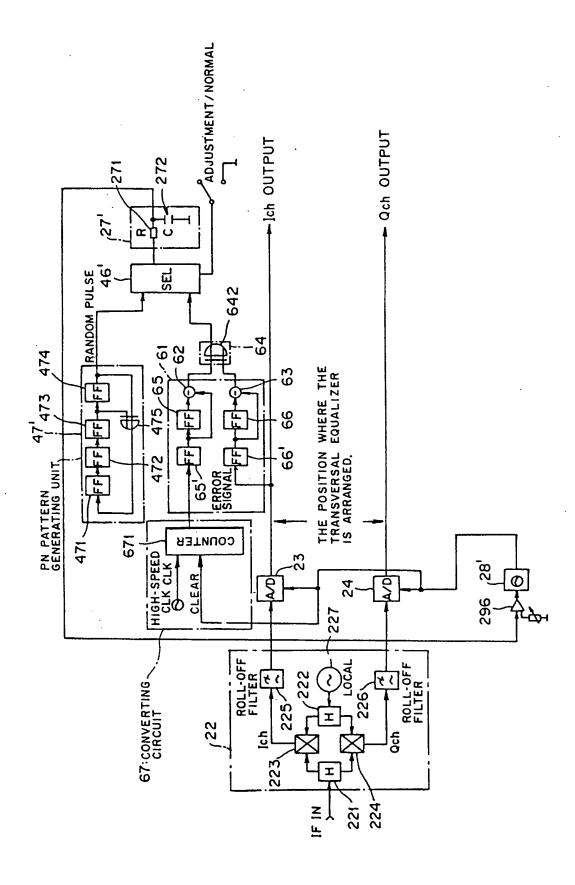
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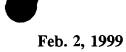


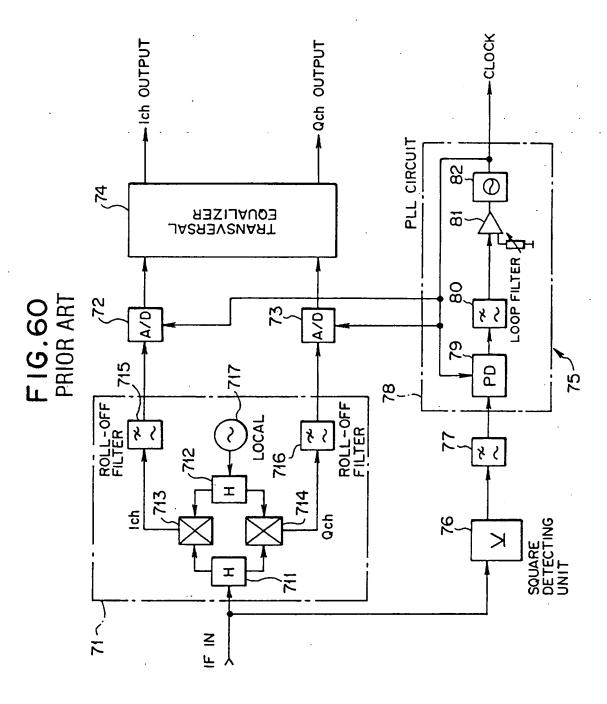
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F16.58









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IDENTIFIER CL_K DATA REGENERATING UNIT EQUALIZER FIG. 61 PRIOR ART 821

DEMODULATOR